CLAIMS

What is claimed is:

1. An integrated circuit, comprising:

a substrate;

at least one area of dielectric material disposed on said substrate;

at least one area of metal material disposed on said substrate;

a bondpad associated with said at least one area of dielectric material and said at least one area of metal material;

a circuitry for generating a negative capacitance, said circuitry generating said negative capacitance of a value to compensate for a capacitance associated with said bondpad, said active circuitry being coupled to said bondpad.

2. The integrated circuit as claimed in claim 1, wherein a value of said negative capacitance is approximately equal in magnitude to said capacitance associated with said bondpad.

3. The integrated circuit as claimed claim 1, wherein said circuitry comprises:

at least two transistors;

at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors;

a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

4. The integrated circuit as claimed in claim 3, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and gallium arsenide pseudomorphic high-electron mobility transistors.

5. The integrated circuit as claimed in claim 3, wherein said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

6. The integrated circuit as claimed in claim 1, wherein said circuitry is fabricated within the substrate.

7. An apparatus, comprising:

a housing;

a substrate disposed within said housing;

at least one area of dielectric material disposed on said substrate;

at least one area of metal material disposed on said substrate;

a bondpad associated with said at least one area of dielectric material and said at least one area of metal material, said bondpad being coupled to said housing; and

a circuitry for generating a negative capacitance, said circuitry generating said negative capacitance of a value to compensate for a capacitance associated with said bondpad, said active circuitry being coupled to said bondpad.

8. The apparatus as claimed in claim 7, wherein said value of said negative capacitance is approximately equal in magnitude to said capacitance associated with said bondpad.

9. The apparatus as claimed claim 7, wherein said circuitry comprises:

at least two transistors;

at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors;

a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

10. The apparatus as claimed in claim 9, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and gallium arsenide pseudomorphic high-electron mobility transistors.

11. The apparatus as claimed in claim 9, wherein said negative capacitance generated by said circuitry is dependent upon a component values of said at least two resistors and said capacitor.

12. The apparatus as claimed in claim 11, wherein said negative capacitance generated by said circuitry is dependent upon a ratio of a first resistor to a second resistor multiplied by a value of said capacitor.

13. The apparatus as claimed in claim 7, wherein said circuitry is fabricated within the substrate.

14. An apparatus, comprising:

a housing;

a substrate disposed within said housing;

at least one area of dielectric material disposed on said substrate;

at least one area of metal material disposed on said substrate;

a bondpad associated with said at least one area of dielectric material and said at least one area of metal material, said bondpad being coupled to said housing; and

a circuitry for generating a negative capacitance, said circuitry generating said negative capacitance of a value approximately equal in magnitude to a capacitance associated with said bondpad, said active circuitry being fabricated within said substrate and coupled to said bondpad.

15. The apparatus as claimed claim 14, wherein said circuitry comprises:

at least two transistors;

at least two resistors; each resistor of said at least two resistors being coupled to each of said at least two transistors;

a capacitor coupled to a first transistor of said at least two transistors and a first resistor of said at least two resistors.

16. The apparatus as claimed in claim 15, wherein said at least two transistors are at least one of bipolar transistors, MOSFETS, and gallium arsenide pseudomorphic high-electron mobility transistors.

17. The apparatus as claimed in claim 15, wherein said negative capacitance generated by said circuitry is dependent upon component values of said at least two resistors and said capacitor.

18. The apparatus as claimed in claim 17, wherein said negative capacitance generated by said circuitry is dependent upon a ratio of a first resistor to a second resistor multiplied by a value of said capacitor.

19. An integrated circuit, comprising:

a substrate;

at least one area of dielectric material disposed on said substrate;

at least one area of metal material disposed on said substrate;

a bondpad associated with said at least one area of dielectric material and said at least one area of metal material;

means for generating a negative capacitance, said generating means generating said negative capacitance of a value to compensate for a capacitance associated with said bondpad.

20. The integrated circuit as claimed in claim 19, wherein said value of said negative capacitance is approximately equal in magnitude to said capacitance associated with said bondpad.